ABSTRACT OF THE DISCLOSURE

A processor element, structured to execute a 32-bit fixed length instruction set architecture, is backward compatible with a 16-bit fixed length instruction set architecture by translating each of the 16-bit instructions into a sequence of one or more 32-bit instructions. Switching between 16-bit instruction execution and 32-bit instruction execution is accomplished by branch instructions that employ a least significant bit position of the address of the target of the branch to identify whether the target instruction is a 16-bit instruction or a 32-bit instruction.